CH7055A Triple High Speed Video DAC

FEATURES

- Three 10-bit high speed DACs
- Sampling frequency up to 200 MHz
- DAC output current range: 2.0 mA to 36 mA
- Wide range of input resolutions support for up to 1920x1200@75Hz (i.e. 640x480, 800x600, 1024x768, 1280x1024, 1600x1200 and etc.)
- Composite Sync Control input
- Composite Sync output
- Sync on Green mode support
- Analog video outputs compliant with VESA VSIS v1r2 specification
- Power-down mode support
- Contrast and Brightness adjustment support
- Serial programmable interface support
- IO Supply Voltages from 1.8V to 3.3V
- Offered in a 40-pin QFN package

APPLICATION

- Car Entertainment Devices
- PC video cards
- High resolution image processing
- Digital video systems
- General purpose high-speed digital-to-analog conversion

GENERAL DESCRIPTION

Chrontel's CH7055A is a low-cost, low-power semiconductor device that consists of three separate 10-bit video Digital-to-Analog Converters (DACs), which can convert the digital input signals into analog current outputs at a maximum conversion rate of 200 MHz.

The DACs are based on current source architecture. Sync and DAC Control Logic module receives horizontal and vertical sync input, generates composite sync and internal synchronization control signal. The CH7055A has a Power-down mode to reduce power consumption as required.

The CH7055A is fabricated in a CMOS process that ensures high functionality with low power dissipation. With advanced Image Enhancement module integrated to achieve the modification of the contrast, brightness, etc, the display quality can be flexible adjusted and optimized through the serial programmable interface.

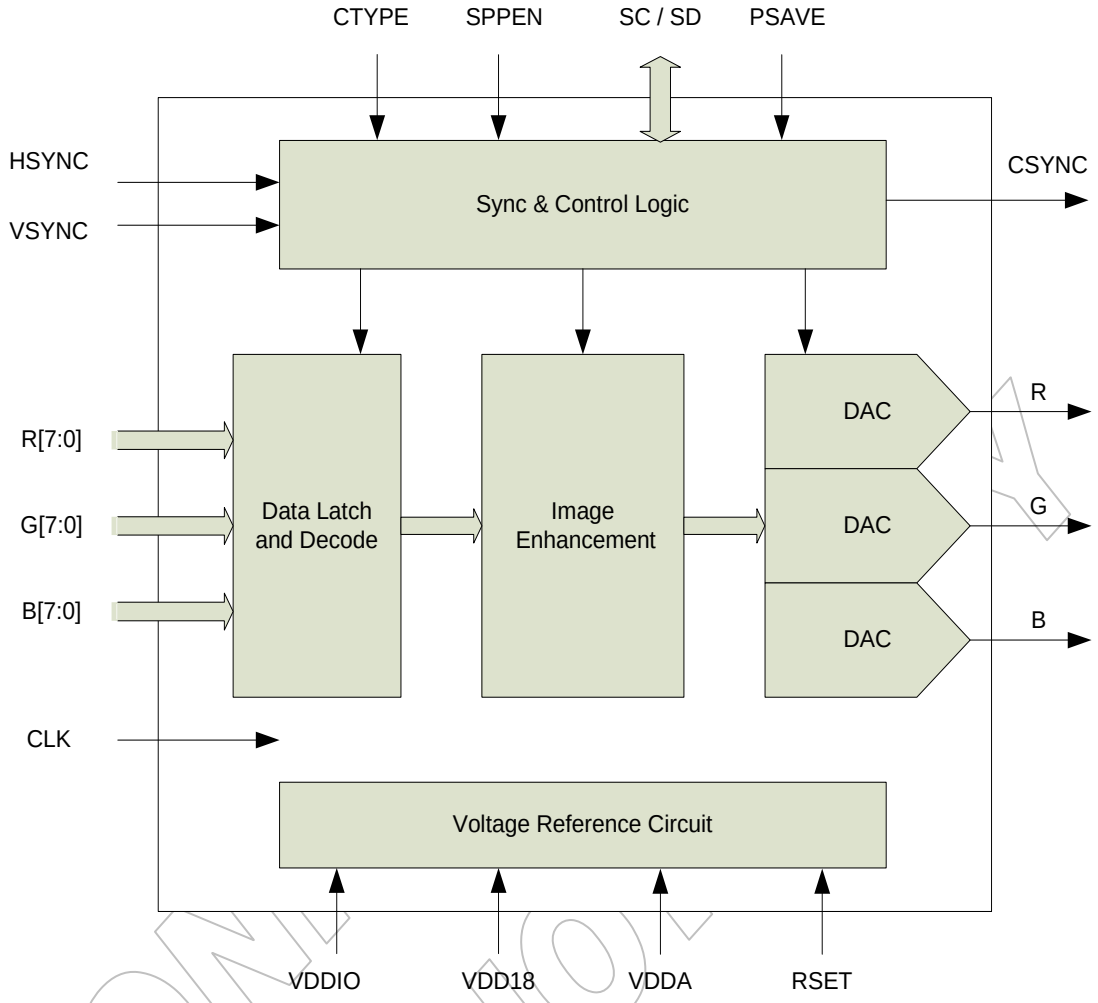

Figure 1: Functional Block Diagram

1.0 PIN-OUT

1.1 Package Diagram

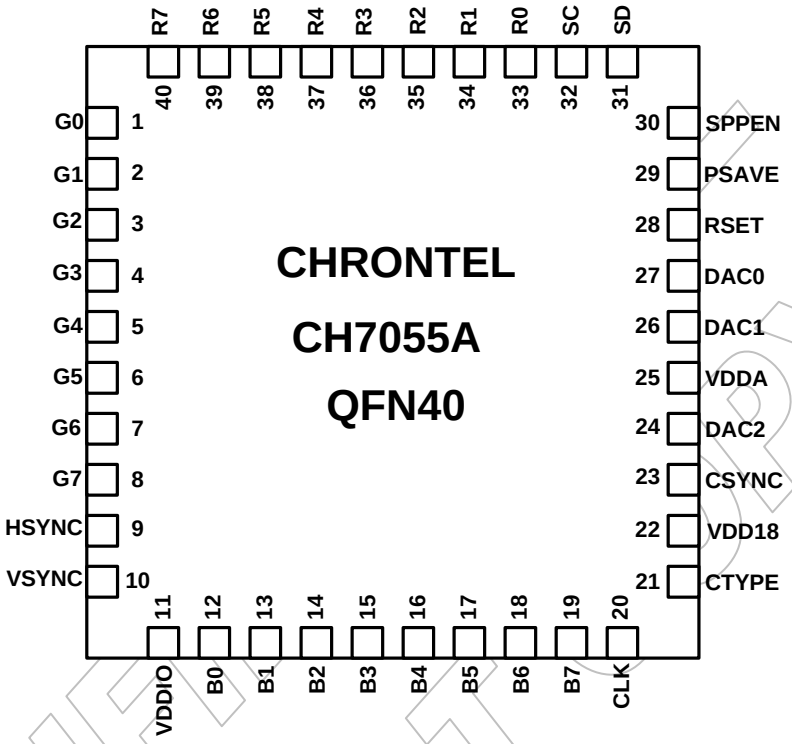

Figure 2: 40 pin QFN Package (Top View)

1.2 Pin Description

Table 1: Pin Name Descriptions (QFN40 Package)

Pin #	Type	Symbol	Description
1~8, 12~19, 33~40,	In	R[7:0] G[7:0] B[7:0]	**Data Input** These pins accept 24 data input lines from a digital video port of a graphics controller. The swing is defined by VDDIO. All the unused Data input pins should be pulled low with 10 KΩ resistors or shorted to Ground directly.
9	In	HSYNC	**Horizontal Sync Input** This pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO.
10	In	VSYNC	**Vertical Sync Input** This pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO.
20	In	CLK	**External Clock Inputs** The input is the clock signal input to the device for use with the H, V, Digital RGB data.
21	In	CTYPE	**Csync Type Select or as DE** When SPPEN =0 CTYPE is Csync Type Select '0': And Gate; '1': XOR Gate Internally pull high and XOR Gate is default When SPPEN=1 CTYPE is connected to DE
23	Out	CSYNC	**Composite sync output** The amplitude of this pin is from 0 to AVDD.
24	Out	DAC2	**Analog RGB output** Full swing is up to 1.3V
26	Out	DAC1	**Analog RGB output** Full swing is up to 1.3V
27	Out	DAC0	**Analog RGB output** Full swing is up to 1.3V
28	In	RSET	**Current Set Resistor Input** This pin sets the DAC current. A 1.2 KΩ, 1% tolerance resistor should be connected between this pin and GND using short and wide traces.
29	In	PSAVE	**Power Saving Mode Enable** Power Save Control. Reduced power consumption is available when this pin is active. Active low.
30	In	SPPEN	**Serial Port Programming Enable** This pin is pull up internally, and should be set active before configure the Chip through the serial port. Active High.
31	I/O	SPD	**Serial Port Data to Input/Output** This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 KΩ resister is required.
32	In	SPC	**Serial Port Clock input** This pin functions as the clock pin of the serial port. External pull-up 6.8 KΩ resister is required.
11	Power	VDDIO	**IO Power Supply (1.8-3.3V)**
22	Power	VDD18	**Digital Power Supply (1.8V)**
25	Power	VDDA	**Analog Power Supply (3.3V)**
Thermal Pad	Power	GND	**Ground**

2.0 PACKAGE DIMENSIONS

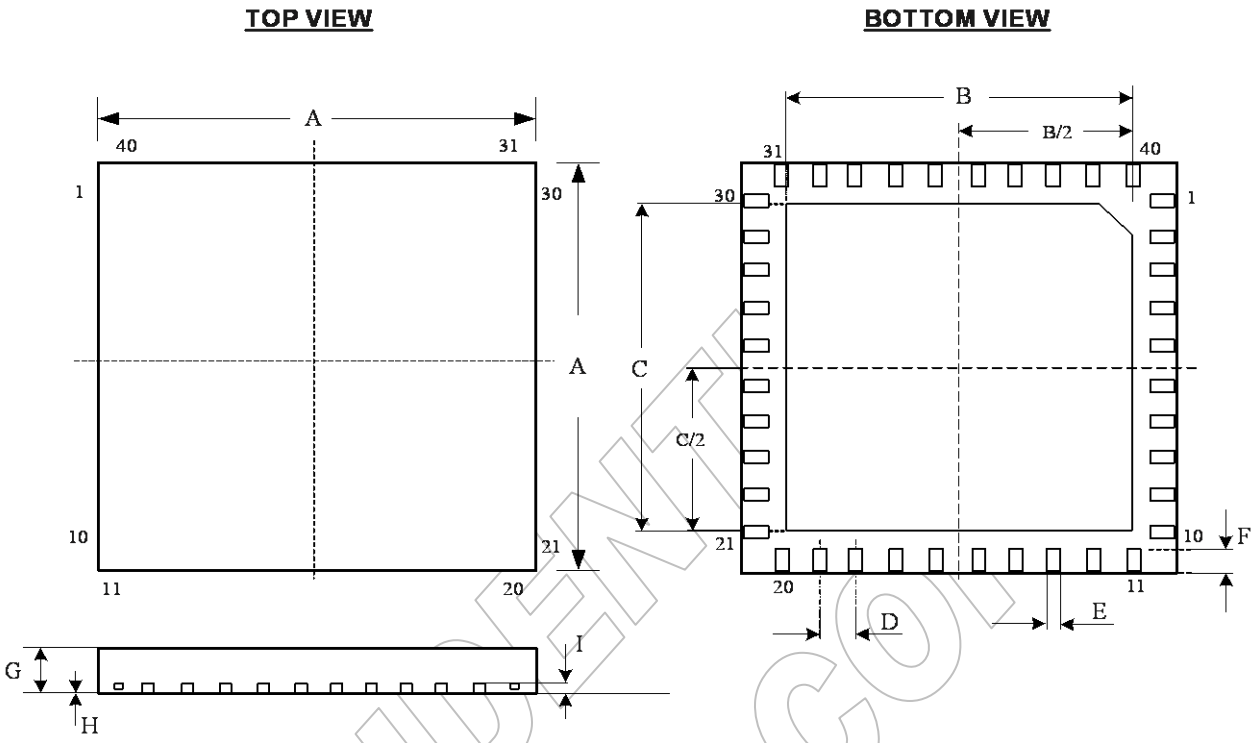

Figure 3: 40 Pin QFN Package (5 x 5 mm)

Table of Dimensions

No. of Leads		SYMBOL								
40 (5 X 5 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	4.90	3.20	3.20	0.4	0.15	0.35	0.7	0	0.20
	MAX	5.10	3.75	3.75		0.25	0.55	0.8	0.05	0.203

Notes:

1. Conforms to JEDEC standard JESD-30 MO-220.

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ORDERING INFORMATION

Part Number	Package Type	Operating Temperature Range	Minimum Order Quantity
CH7055A-BF	40QFN, Lead-free	Commercial : -20 to 70°C	490/Tray
CH7055A-BFI	40QFN, Lead-free	Industrial : -40 to 85°C	490/Tray

Chrontel

Chrontel International Limited

129 Front Street, 5th floor,

Hamilton, Bermuda HM12

www.chrontel.com
E-mail: sales@chrontel.com